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Modeling Guidelines for Code Generation



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R2020a



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Modeling Guidelines for Code Generation

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March 2012	Online only	Revised for Version 1.3 (Release 2012a)
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Introduction

- “Motivation” on page 1-2
- “Guideline Template” on page 1-3

Motivation

MathWorks intends the guidelines for engineers developing models and generating code for embedded systems using Model-Based Design with MathWorks products. The guidelines provide recommendations for model settings, block usage, and block parameters that impact simulation behavior or code generated by the Embedded Coder® product.

The guidelines do not address model style or development processes. For more information about creating models in a way that improves consistency, clarity, and readability, see the “MAB Modeling Guidelines”. Development process guidance and additional information for specific standards is available with the IEC Certification Kit (for ISO 26262 and IEC 61508) and DO Qualification Kit (for DO-178) products.

Disclaimer While adhering to the recommendations in the guidelines will reduce the risk that an error is introduced during development and not be detected, it is not a guarantee that the system being developed will be safe. Conversely, if some of the recommendations in the guidelines are not followed, it does not mean that the system being developed will be unsafe.

Guideline Template

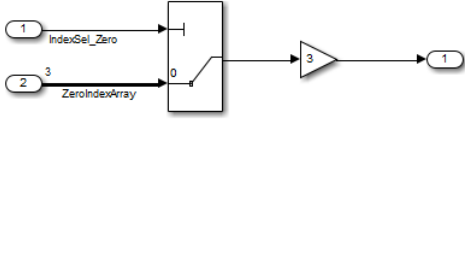
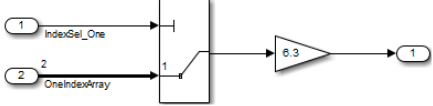
Guideline descriptions are documented, using the following template. Companies that want to create additional guidelines are encouraged to use the same template.

ID: Title	<i>XX_nnnn</i> : Title of the guideline (unique, short)
Description	Description of the guideline
Prerequisites	Links to guidelines that are prerequisites to this guideline (ID: Title)
Notes	Notes for using the guideline
Rationale	Rationale for providing the guideline
Model Advisor Check	Title of and link to the corresponding Model Advisor check, if a check exists
References	References to standards that apply to guideline
See Also	Links to additional information
Last Changed	Version number of last change
Examples	Guideline examples

Block Considerations

- “cgsl_0101: Zero-based indexing” on page 2-2
- “cgsl_0102: Evenly spaced breakpoints in lookup tables” on page 2-3
- “cgsl_0103: Precalculated signals and parameters” on page 2-4
- “cgsl_0104: Modeling global shared memory using data stores” on page 2-7
- “cgsl_0105: Modeling local shared memory using data stores” on page 2-10

cgsl_0101: Zero-based indexing

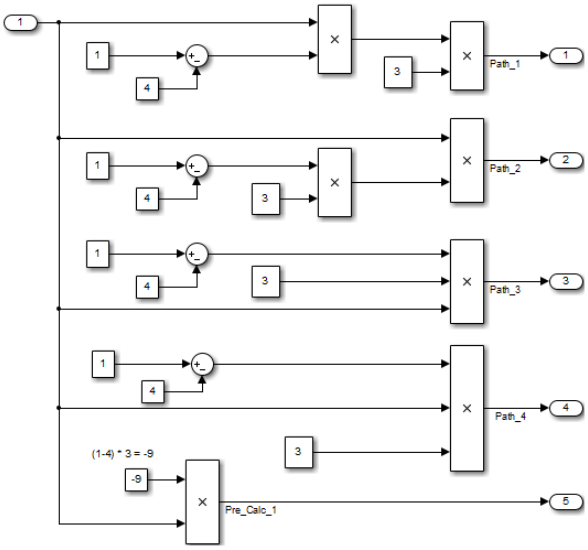
ID: Title	cgsl_0101: Zero-based indexing	
Description	Use zero-based indexing for blocks that require indexing. To set up zero-based indexing, do one of the following:	
	A	Select the Index Vector block parameter Use zero-based contiguous .
	B	Set block parameter Index mode to Zero-based for the following blocks: <ul style="list-style-type: none"> • Assignment • Selector • For Iterator • Find Nonzero Elements
Notes	The C language uses zero-based indexing.	
Rationale	A, B	Use zero-based indexing for compatibility with integrated C code.
	A, B	Results in more efficient C code execution. One-based indexing requires a subtraction operation in generated code.
See Also	"hisl_0021: Consistent vector indexing method"	
Last Changed	R2011b	
Examples	 <p>Recommended</p> <pre>void ZeroIndex(void) { Y.Out5 = 3.0 * ZeroIndexArray[IndexSel_Zero]; }</pre>	
	 <p>Not Recommended</p> <pre>void OneIndex(void) { Y.Out1 = OneIndexArray[IndexSel_One - 1] * 6.3; }</pre>	

cgsl_0102: Evenly spaced breakpoints in lookup tables

ID: Title	cgsl_0102: Evenly spaced breakpoints in lookup tables	
Description	When you use Lookup Table and Prelookup blocks,	
	A	With <i>non-fixed-point data types</i> , use evenly spaced data breakpoints for the input axis
	B	With <i>fixed-point data types</i> , use power of two spaced breakpoints for the input axis
Notes	Evenly spaced breakpoints can prevent generated code from including division operations, resulting in faster execution.	
Rationale	A	Improve ROM usage and execution speed.
	B	<p>Improve execution speed.</p> <p>When compared to unevenly spaced data, power-of-two data can</p> <ul style="list-style-type: none"> • Increase data RAM usage if you require a finer step size • Reduce accuracy if you use a coarser step size <p>Compared to an evenly spaced data set, there should be minimal cost in memory or accuracy.</p>
Model Advisor Checks	By Product > Embedded Coder > Identify questionable fixed-point operations	
	For check details, see “Identify questionable fixed-point operations” (Embedded Coder).	
See Also	“Formulation of Evenly Spaced Breakpoints” in the Simulink documentation	
Last Changed	R2010b	

cgsl_0103: Precalculated signals and parameters

ID: Title	cgsl_0103: Precalculated signals and parameters	
Description	Precalculate invariant parameters and signals by doing one of the following:	
	A	Manually precalculate the values
	B	Set these configuration parameters: <ul style="list-style-type: none"> • Set Default parameter behavior to Inlined • Select Inline invariant signals
Notes	Precalculating variables can reduce local and global memory usage and improve execution speed. If you set Default parameter behavior to Inlined and enable Inline invariant signals , the code generator minimizes the number of run-time calculations by maximizing the number calculations completed before run time. In some cases, this can lead to a reduction in the number of parameters stored. However, the algorithms the code generator uses have limitations. In some cases, the code is more compact if you calculate the values outside of the Simulink environment. This can improve model efficiency, but can reduce model readability.	
Rationale	A, B	Precalculate data, outside of the Simulink environment, to reduce memory requirements of a system and improve run-time execution.
Last Changed	R2012b	

ID: Title	cgs1_0103: Precalculated signals and parameters
Examples	<p>In the following model, the four paths are mathematically equivalent. However, due to algorithm limitations, the number of run-time calculations for the paths differs.</p>  <pre> Path_1 = InputSignal * -3.0 * 3.0; /* Product: '<Root>/Product4' incorporates: * Inport: '<Root>/In1' */ Path_2 = InputSignal * -9.0; /* Product: '<Root>/Product2' incorporates: * Constant: '<Root>/Constant2' * Inport: '<Root>/In1' */ Path_3 = -9.0 * InputSignal; /* Product: '<Root>/Product5' incorporates: * Constant: '<Root>/Constant2' * Inport: '<Root>/In1' */ Path_4 = -3.0 * InputSignal * 3.0; /* Product: '<Root>/Product6' incorporates: * Constant: '<Root>/Constant3' * Inport: '<Root>/In1' */ Pre_Calc_1 = -9.0 * InputSignal; </pre> <p>To maximize automatic precalculation, add signals at the end of the set of equations.</p> <p>Inlining data reduces the ability to tune model parameters. You should define parameters that require calibration to allow calibration. For more</p>

ID: Title	cgsI_0103: Precalculated signals and parameters
	information, see “Create Tunable Calibration Parameter in the Generated Code” (Simulink Coder).

cgsl_0104: Modeling global shared memory using data stores

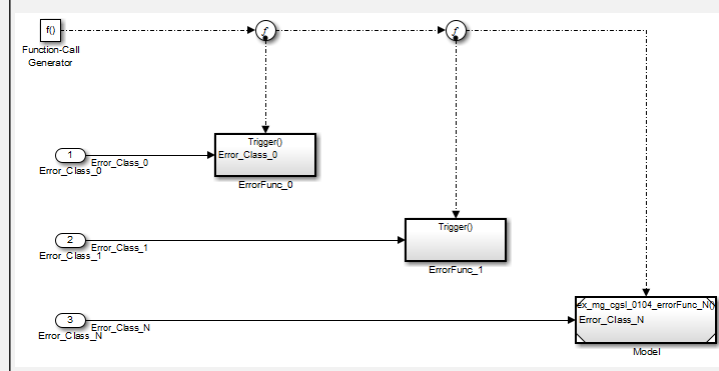
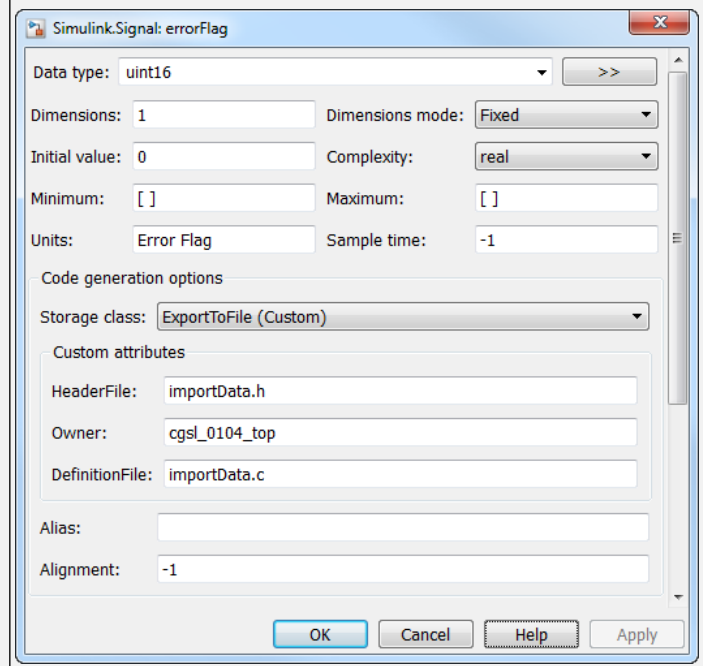
ID: Title	cgsl_0104: Modeling global shared memory using data stores	
Description	When using data store blocks to model shared memory across multiple models:	
	A	Set configuration parameters Duplicate data store names to error for models in the hierarchy.
	B	Define the data store using a Simulink Signal or MPT Signal object.
	C	Do not use Data Store Memory blocks in the model.
Notes	<p>If multiple Data Store blocks use the same data store name within a model, then Simulink interprets each instance of the data store as having a unique local scope.</p> <p>Use Duplicate data store names to help detect unintended identifier reuse. For models intentionally using local data stores, set the diagnostic to warning. Verify that only intentional data stores are included.</p> <p>Merge blocks, used in conjunction with subsystems operating in a mutually exclusive manor, provide a second method of modeling global data across multiple models.</p>	
Rationale	A, B, C	Promotes a modeling pattern where a single consistent data store is used across models and a single global instance is created in the generated code.
See Also	<ul style="list-style-type: none"> • “hisl_0013: Usage of data store blocks” • “hisl_0015: Usage of Merge blocks” • “cgsl_0302: Diagnostic settings for multirate and multitasking models” on page 4-3 • “cgsl_0105: Modeling local shared memory using data stores” on page 2-10 	
Last Changed	R2011b	

ID: Title **cgsl_0104: Modeling global shared memory using data stores**

Examples

The following examples illustrate the use of data stores as global shared memory. The data store is used to model a global fault flag. A data store is required because the flag can be set in multiple functions and used in the same execution step.

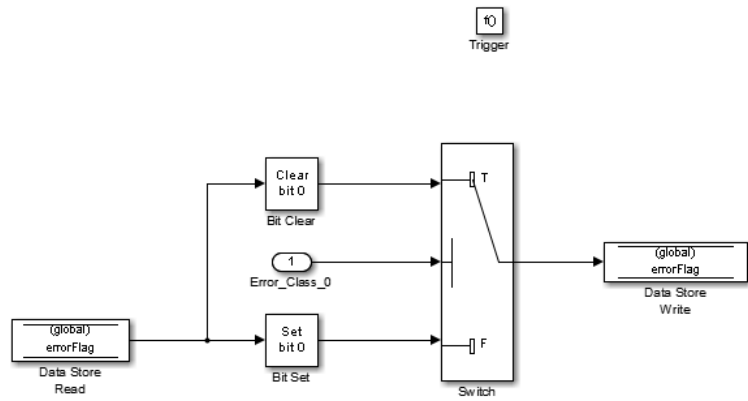
The top model contains three subsystems, each utilizing a data store memory. The data store is defined using a signal data object.



Recommended

In this example, there are no Data Store Memory blocks. The resulting code uses the same global variable for the full model.

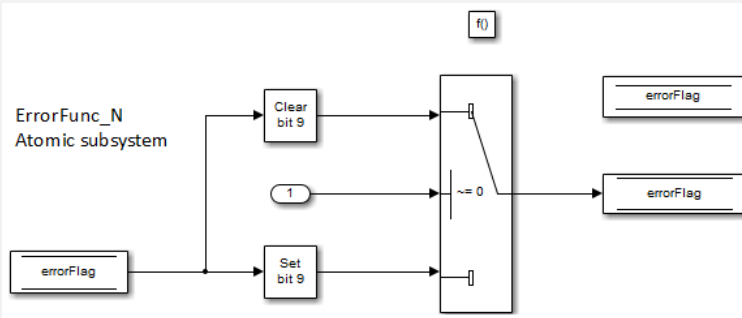
ID: Title cgsl_0104: Modeling global shared memory using data stores



```
void cgsl_0104_top_ErrorFunc_0(void)
{
  if (Error_Class_0) {
    errorFlag = (uint16_T) (~((uint16_T) ((uint16_T) (~errorFlag) | ((uint16_T) 1U))));
  } else {
    errorFlag = (uint16_T) (errorFlag | ((uint16_T) 1U));
  }
}
```

Not Recommended

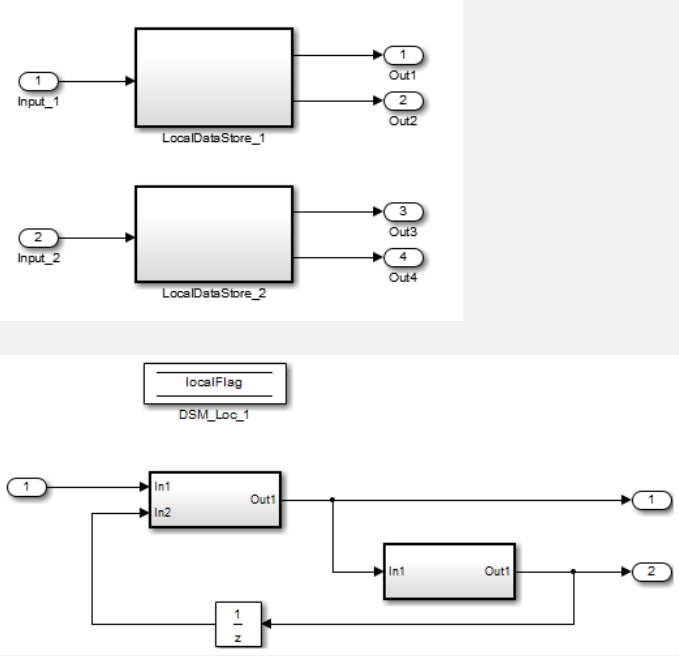
In this example, a Data Store Memory block is added into the Model block subsystem. The model subsystem uses a local version of the data store. The Atomic Subsystem use a different version.



```
rtMdlrefDWorK_mr_cgsl_0104_errro_mr_cgsl_0104_errorF_MdlrefDWorK;
void mr_cgsl_0104_errorFunc_N_UseDSM(const boolean_T *rtu_Error_Class_N)
{
  rtDW_mr_cgsl_0104_errorFunc_N_U *localDW =
    &(mr_cgsl_0104_errorF_MdlrefDWorK.rtdw);
  if (*rtu_Error_Class_N) {
    localDW->errorFlag = (uint16_T) (~((uint16_T) ((uint16_T) (~localDW->errorFlag)
      | ((uint16_T) 512U))));
  } else {
    localDW->errorFlag = (uint16_T) (localDW->errorFlag | ((uint16_T) 512U));
  }
}
```

cgsl_0105: Modeling local shared memory using data stores

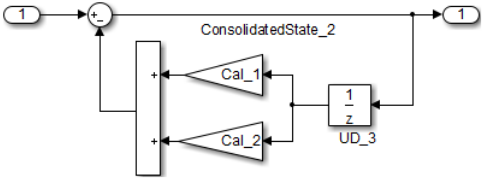
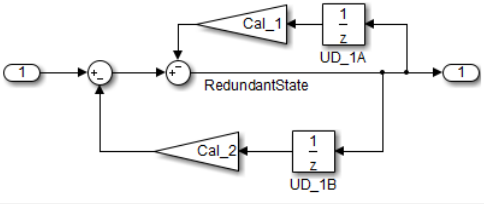
ID: Title	cgsl_0105: Modeling local shared memory using data stores	
Description	When using data store blocks as local shared memory:	
	A	Explicitly create the data store using a Data Store Memory block.
	B	Clear block parameter Data store name must resolve to Simulink signal object.
	C	Consider following a naming convention for local Data Store Memory blocks.
Notes	<p>Use configuration parameter Duplicate data store names to help detect unintended identifier reuse. For models intentionally using local data stores, set the diagnostic to warning. Verify that only intentional data stores are included.</p> <p>Data store blocks are realized as global memory in the generated code. If they are not assigned a specific storage class, they are included in the DWork structure. In the model, the data store is scoped to the defining subsystem and below. In the generated code, the data store has file scope.</p>	
Rationale	A, B	Data store block is treated as a local instance of the data store
	C	Provides graphical feedback that the data store is local
See Also	<ul style="list-style-type: none"> • “cgsl_0104: Modeling global shared memory using data stores” on page 2-7 • “cgsl_0302: Diagnostic settings for multirate and multitasking models” on page 4-3 • “hisl_0013: Usage of data store blocks” 	
Last Changed	R2011b	

ID: Title	cgsl_0105: Modeling local shared memory using data stores
Examples	<p>In some instances, such as a library function, reuse of a local data store is required. In this example, the local data store is defined in two subsystems.</p>  <p>The diagram illustrates two subsystems, LocalDataStore_1 and LocalDataStore_2, each with its own local data store. LocalDataStore_1 has an input 'Input_1' (labeled '1') and two outputs 'Out1' (labeled '1') and 'Out2' (labeled '2'). LocalDataStore_2 has an input 'Input_2' (labeled '2') and two outputs 'Out3' (labeled '3') and 'Out4' (labeled '4'). Below this, a larger subsystem is shown with a data store 'localFlag' (DSM_Loc_1). It contains two blocks: one with inputs 'In1' and 'In2' and output 'Out1', and another with input 'In1' and output 'Out1'. A signal '1' enters from the left, goes to 'In1' of the first block, and also to 'In2' of the second block. The output 'Out1' of the first block goes to 'In1' of the second block. The output 'Out1' of the second block goes to a block labeled '1/z'. The output of '1/z' goes back to 'In2' of the first block. The output of the first block also goes to an output '1' on the right, and the output of the second block goes to an output '2' on the right.</p> <p>The instance of localFlag is in scope within the subsystem LocalDataStore_1 and its subsystems.</p> <pre data-bbox="584 1197 1291 1312"> /* Block signals and states (auto storage) for system '<Root>' */ typedef struct { real_T localFlag; /* '<S2>/DSM_Loc_2' */ real_T localFlag_k; /* '<S1>/DSM_Loc_1' */ } D_Work_cgsl_0105; </pre> <p>In the generated code, the data stores are part of the global DWork structure for the model. Embedded Coder automatically assigns them unique names during the code generation process.</p>

Modeling Pattern Considerations

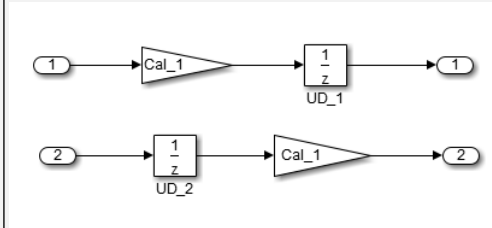
- “cgsl_0201: Redundant Unit Delay and Memory blocks” on page 3-2
- “cgsl_0202: Usage of For, While, and For Each subsystems with vector signals” on page 3-6
- “cgsl_0204: Vector and bus signals crossing into atomic subsystems or Model blocks” on page 3-7
- “cgsl_0205: Signal handling for multirate models” on page 3-12
- “cgsl_0206: Data integrity and determinism in multitasking models” on page 3-14

cgsl_0201: Redundant Unit Delay and Memory blocks

ID: Title	cgsl_0201: Redundant Unit Delay and Memory blocks	
Description	When preparing a model for code generation, A Remove redundant Unit Delay and Memory blocks.	
Rationale	A	Redundant Unit Delay and Memory blocks use additional global memory. Removing the redundancies from a model reduces memory usage without impacting model behavior.
Last Changed	R2013a	
Example	 <p>Recommended: Consolidated Unit Delays</p> <pre data-bbox="354 884 1136 1003"> void Reduced(void) { ConsolidatedState_2 = Matrix_UD_Test - (Cal_1 * DWork.UD_3_DSTATE + Cal_2 * DWork.UD_3_DSTATE); DWork.UD_3_DSTATE = ConsolidatedState_2; } </pre>	
	 <p>Not Recommended: Redundant Unit Delays</p> <pre data-bbox="354 1310 1104 1453"> void Redundant(void) { RedundantState = (Matrix_UD_Test - Cal_2 * DWork.UD_1B_DSTATE) - Cal_1 * DWork.UD_1A_DSTATE; DWork.UD_1B_DSTATE = RedundantState; DWork.UD_1A_DSTATE = RedundantState; } </pre>	

ID: Title cgsl_0201: Redundant Unit Delay and Memory blocks

Unit Delay and Memory blocks exhibit commutative and distributive algebraic properties. When the blocks are part of an equation with one driving signal, you can move the Unit Delay and Memory blocks to a new position in the equation without changing the result.



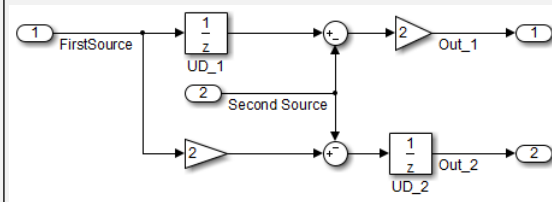
For the top path in the preceding example, the equations for the blocks are:

- 1 $Out_1(t) = UD_1(t)$
- 2 $UD_1(t) = In_1(t-1) * Cal_1$

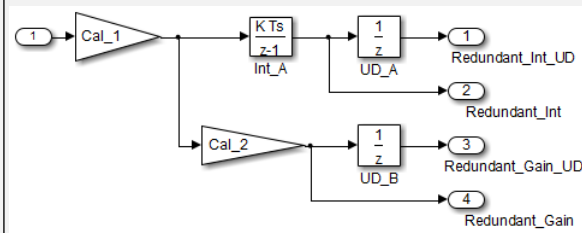
For the bottom path, the equations are:

- 1 $Out_2(t) = UD_2(t) * Cal_1$
- 2 $UD_2(t) = In_2(t-1)$

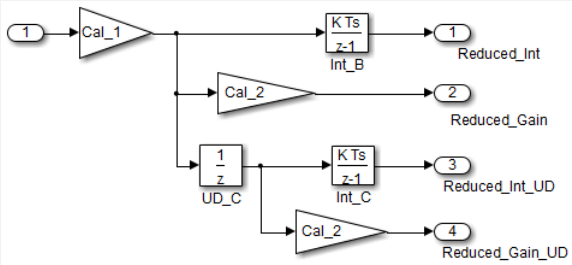
In contrast, if you add a secondary signal to the equations, the location of the Unit Delay block impacts the result. As the following example shows, the location of the Unit Delay block impacts the results due to the skewing of the time sample between the top and bottom paths.



In cases with a single source and multiple destinations, the comparison is more complex. For example, in the following model, you can refactor the two Unit Delay blocks into a single unit delay.



ID: Title **cgsl_0201: Redundant Unit Delay and Memory blocks**



From a black box perspective, the two models are equivalent. However, from a memory and computation perspective, differences exist between the two models.

```

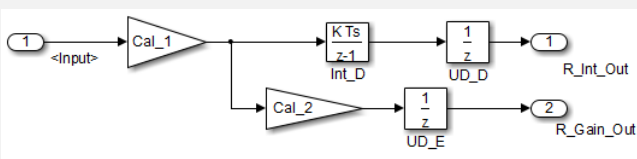
{
  real_T rtb_Gain4;
  rtb_Gain4 = Cal_1 * Redundant;
  Y.Redundant_Gain = Cal_2 * rtb_Gain4;
  Y.Redundant_Int = DWork.Int_A;
  Y.Redundant_Int_UD = DWork.UD_A;
  Y.Redundant_Gain_UD = DWork.UD_B;
  DWork.Int_A = 0.01 * rtb_Gain4 + DWork.Int_A;
  DWork.UD_A = Y.Redundant_Int;
  DWork.UD_B = Y.Redundant_Gain;
}

{
  real_T rtb_Gain1;
  real_T rtb_UD_C;
  rtb_Gain1 = Cal_1 * Reduced;
  rtb_UD_C = DWork.UD_C;
  Y.Reduced_Gain_UD = Cal_2 * DWork.UD_C;
  Y.Reduced_Gain = Cal_2 * rtb_Gain1;
  Y.Reduced_Int = DWork.Int_B;
  Y.Reduced_Int_UD = DWork.Int_C;
  DWork.UD_C = rtb_Gain1;
  DWork.Int_B = 0.01 * rtb_Gain1 + DWork.Int_B;
  DWork.Int_C = 0.01 * rtb_UD_C + DWork.Int_C;
}

```

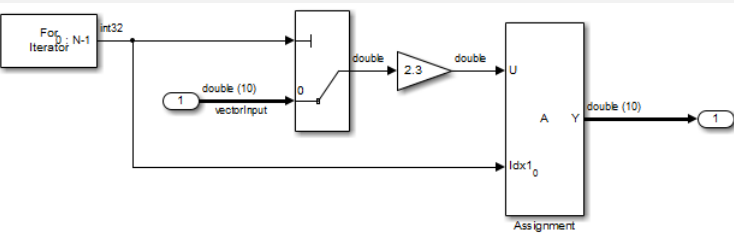
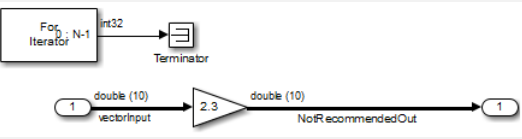
In this case, the original model is more efficient. In the first code example, there are three global variables, two from the Unit Delay blocks (DWork.UD_A and DWork.UD_B) and one from the discrete time integrator (DWork.Int_A). The second code example shows a reduction to one global variable generated by the unit delays (Dwork.UD_C), but there are two global variables due to the redundant Discrete Time Integrator blocks (DWork.Int_B and DWork.Int_C). The Discrete Time Integrator block path introduces an additional local variable (rtb_UD_C) and two additional computations.

By contrast, the refactored model (second) below is more efficient.



ID: Title	cgs1_0201: Redundant Unit Delay and Memory blocks
	<pre> { real_T rtb_Gain4_f; real_T rtb_Int_D; rtb_Gain4_f = Cal_1 * U.Input; rtb_Int_D = DWork.Int_D; Y.R_Int_Out = DWork.UD_D; Y.R_Gain_Out = DWork.UD_E; DWork.Int_D = 0.01 * rtb_Gain4_f + DWork.Int_D; DWork.UD_D = rtb_Int_D; DWork.UD_E = Cal_2 * rtb_Gain4_f; } { real_T rtb_UD_F; rtb_UD_F = DWork.UD_F; Y.Gain_Out = Cal_2 * DWork.UD_F; Y.Int_Out = DWork.Int_E; DWork.UD_F = Cal_1 * U.Input; DWork.Int_E = 0.01 * rtb_UD_F + DWork.Int_E; } </pre> <p>The code for the refactored model is more efficient because the branches from the root signal do not have a redundant unit delay.</p>

cgsl_0202: Usage of For, While, and For Each subsystems with vector signals

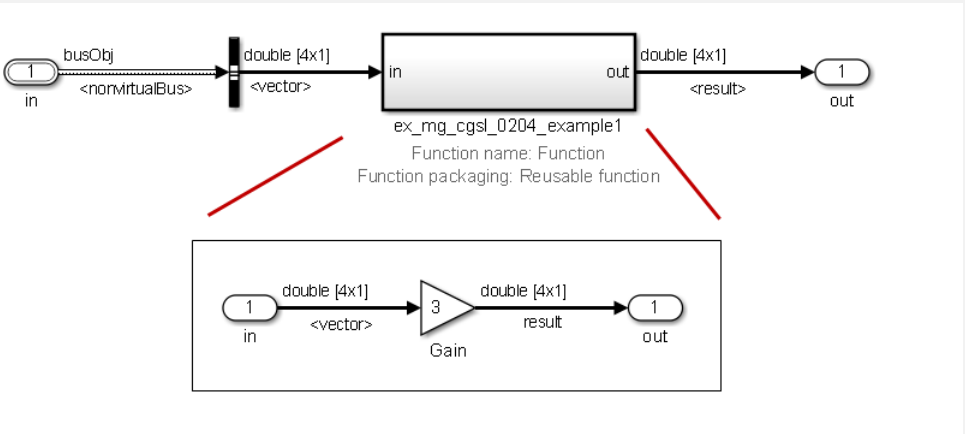
ID: Title	cgsl_0202: Usage of For, While, and For Each subsystems with vector signals	
Description	A	Use For, While, and For Each subsystems for calculations that require iterative behavior or operate on a subset (frame) of data.
	B	Avoid using For, While, or For Each subsystems for basic vector operations.
Rationale	A, B	Avoid redundant loops.
See Also	<ul style="list-style-type: none"> “Loop unrolling threshold” (Simulink Coder) in the Simulink documentation 	
Last Changed	R2010b	
Examples	<p>The recommended method for preceding calculation is to place the Gain block outside the For Subsystem. If the calculations are required as part of a larger algorithm, you can avoid the nesting of for loops by using Index Vector and Assignment blocks.</p>  <p>Recommended</p> <pre>for (s1_iter = 0; s1_iter < 10; s1_iter++) { RecommendedOut[s1_iter] = 2.3 * vectorInput[s1_iter]; }</pre> <p>A common mistake is to embed basic vector operations in a For, While, or For Each subsystem. The following example includes a simple vector gain inside a For subsystem, which results in unnecessary nested for loops.</p>  <p>Not Recommended</p> <pre>for (s1_iter = 0; s1_iter < 10; s1_iter++) { for (i = 0; i < 10; i++) { NotRecommendedOut[i] = 2.3 * vectorInput[i]; } }</pre>	

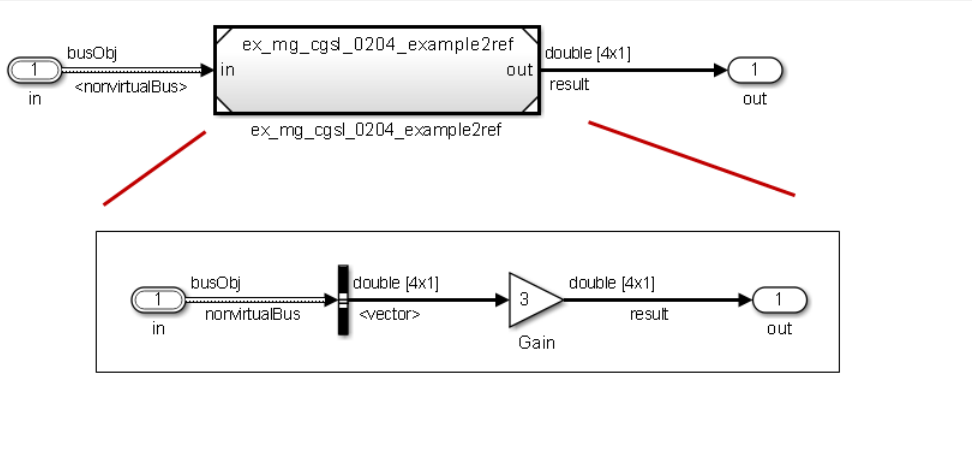
cgsi_0204: Vector and bus signals crossing into atomic subsystems or Model blocks

ID: Title	cgsi_0204: Vector and bus signals crossing into atomic subsystems or Model blocks																																					
Description	When working with vector or bus signals and some of the signal elements are in an atomic subsystem or a referenced model, use the following information to determine how to select signal elements to minimize memory usage.																																					
	A	<p>Bus or vector entering an atomic subsystem:</p> <table border="1" data-bbox="555 619 1474 1056"> <thead> <tr> <th colspan="3" data-bbox="555 619 1474 667">Function packaging: Non-reusable function</th> </tr> <tr> <th colspan="3" data-bbox="555 667 1474 716">Function interface: void_void</th> </tr> <tr> <th data-bbox="555 716 857 829"></th> <th data-bbox="857 716 1170 829">Signals selected outside subsystem results in...</th> <th data-bbox="1170 716 1474 829">Signal selected inside subsystem results in...</th> </tr> </thead> <tbody> <tr> <td data-bbox="555 829 857 871">Virtual Bus</td> <td data-bbox="857 829 1170 871">No data copies.</td> <td data-bbox="1170 829 1474 871">No data copies.</td> </tr> <tr> <td data-bbox="555 871 857 913">Nonvirtual Bus</td> <td data-bbox="857 871 1170 913">No data copies.</td> <td data-bbox="1170 871 1474 913">No data copies.</td> </tr> <tr> <td data-bbox="555 913 857 1056">Vector</td> <td data-bbox="857 913 1170 1056">A copy of the selected signals in global block I/O structure that is used in the function.</td> <td data-bbox="1170 913 1474 1056">No data copies.</td> </tr> </tbody> </table> <table border="1" data-bbox="555 1066 1474 1661"> <thead> <tr> <th colspan="3" data-bbox="555 1066 1474 1115">Function packaging: Non-reusable function</th> </tr> <tr> <th colspan="3" data-bbox="555 1115 1474 1163">Function interface: Allow arguments (Optimized)</th> </tr> <tr> <th data-bbox="555 1163 857 1276"></th> <th data-bbox="857 1163 1170 1276">Signals selected outside subsystem results in</th> <th data-bbox="1170 1163 1474 1276">Signal selected inside subsystem results in</th> </tr> </thead> <tbody> <tr> <td data-bbox="555 1276 857 1415">Virtual Bus</td> <td data-bbox="857 1276 1170 1415">No data copies. Only the selected signals are passed to the function.</td> <td data-bbox="1170 1276 1474 1415">No data copies. Only the selected signals are passed to the function.</td> </tr> <tr> <td data-bbox="555 1415 857 1528">Nonvirtual Bus</td> <td data-bbox="857 1415 1170 1528">No data copies. Only the selected signals are passed to the function.</td> <td data-bbox="1170 1415 1474 1528">No data copies. The whole bus is passed to the function.</td> </tr> <tr> <td data-bbox="555 1528 857 1661">Vector</td> <td data-bbox="857 1528 1170 1661">A copy of the selected signals in a local variable that is passed to the function.</td> <td data-bbox="1170 1528 1474 1661">No data copies. The whole vector is passed to the function.</td> </tr> </tbody> </table>		Function packaging: Non-reusable function			Function interface: void_void				Signals selected outside subsystem results in...	Signal selected inside subsystem results in...	Virtual Bus	No data copies.	No data copies.	Nonvirtual Bus	No data copies.	No data copies.	Vector	A copy of the selected signals in global block I/O structure that is used in the function.	No data copies.	Function packaging: Non-reusable function			Function interface: Allow arguments (Optimized)				Signals selected outside subsystem results in	Signal selected inside subsystem results in	Virtual Bus	No data copies. Only the selected signals are passed to the function.	No data copies. Only the selected signals are passed to the function.	Nonvirtual Bus	No data copies. Only the selected signals are passed to the function.	No data copies. The whole bus is passed to the function.	Vector	A copy of the selected signals in a local variable that is passed to the function.
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ID: Title	cgsl_0204: Vector and bus signals crossing into atomic subsystems or Model blocks		
	Function packaging: Reusable function		
		Signals selected outside subsystem results in	Signal selected inside the subsystem results in
	Virtual Bus	No data copies. Only the selected signals are passed to the function.	No data copies. Only the selected signals are passed to the function.
	Nonvirtual Bus	No data copies. Only the selected signals are passed to the function. See example 1.	No data copies. The whole bus is passed to the function.
	Vector	A copy of the selected signals in a local variable that is passed to the function.	No data copies. The whole vector is passed to the function.

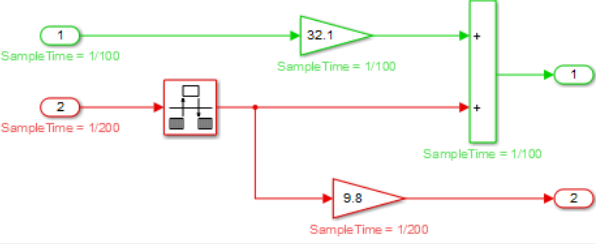
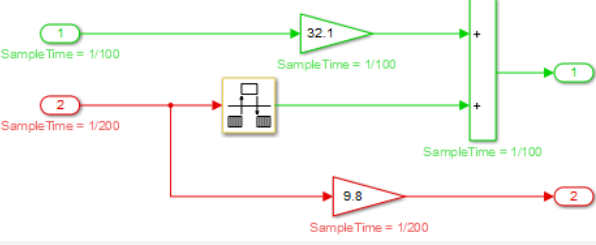
ID: Title		cgs1_0204: Vector and bus signals crossing into atomic subsystems or Model blocks													
	B	Bus or vector entering a Model block:													
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			Signals selected outside Model block results in...	Signal selected inside Model block results in...											
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Vector	A copy of the selected signals in a local variable that is passed to the function.	No data copies. The whole vector is passed to the function.													
Notes	<ul style="list-style-type: none"> Depending on Embedded Coder settings (e.g. optimizations), predecessor blocks and signal storage classes, actual results might differ from the tables. Virtual busses do not support global data. If the subsystem is set to <code>InLine</code>, data copies do not occur. 														
Rationale	A, B	Minimize RAM, ROM, and stack usage													
Last Changed	R2016a														

ID: Title	cgs1_0204: Vector and bus signals crossing into atomic subsystems or Model blocks
Examples	<p>Example 1: Nonvirtual bus entering an atomic subsystem</p> <ul style="list-style-type: none"> • Function packaging: Reusable function • Selection: Subsignal selected outside the subsystem  <p>Only the selected signals are passed to the function:</p> <pre data-bbox="446 987 1136 1270"> 6 void Function(const real_T rtu_in[4], real_T rty_out[4]) 7 { 8 rty_out[0] = 3.0 * rtu_in[0]; 9 rty_out[1] = 3.0 * rtu_in[1]; 10 rty_out[2] = 3.0 * rtu_in[2]; 11 rty_out[3] = 3.0 * rtu_in[3]; 12 } 13 14 void ex_mg_cgs1_0204_example1_step(void) 15 { 16 Function(&nonvirtualBus.vector[0], Y.Out1); 17 } </pre>

ID: Title	cgs1_0204: Vector and bus signals crossing into atomic subsystems or Model blocks
	<p>Example 2: Nonvirtual bus entering a model block</p> <ul style="list-style-type: none"> • Total number of instances allowed per top model: Multiple • Selection: Subsignal selected inside the referenced model  <p>There are no data copies in the code for the main model. The whole bus is passed to the model reference function.</p> <pre data-bbox="456 1045 1338 1140"> 6 void ex_mg_cgs1_0204_example2_step(void) 7 { 8 ex_mg_cgs1_0204_example2ref(&ex_mg_cgs1_0204_example2_U.nonvirtualBus, 9 &ex_mg_cgs1_0204_example2_Y.Out1[0]); </pre> <p>Code for the model reference function:</p> <pre data-bbox="456 1241 1338 1402"> 4 void ex_mg_cgs1_0204_example2ref(const busObj *rtu_in, real_T rty_out[4]) 5 { 6 rty_out[0] = 3.0 * rtu_in->vector[0]; 7 rty_out[1] = 3.0 * rtu_in->vector[1]; 8 rty_out[2] = 3.0 * rtu_in->vector[2]; 9 rty_out[3] = 3.0 * rtu_in->vector[3]; 10 } </pre>

cgsl_0205: Signal handling for multirate models

ID: Title	cgsl_0205: Signal handling for multirate models	
Description	For multirate models, handle the change in operation rate in one of two ways:	
	A	At the destination block, Insert a Rate Transition.
	B	Set configuration parameter Automatically handle rate transition for data transfer to <i>Always</i> or <i>Whenever possible</i> .
Rationale	A,B	Following this guideline supports the handling of data operating at different rates.
Note	<p>Setting Automatically handle rate transition for data transfer to <i>Whenever possible</i> requires you to insert a Rate Transition block in locations indicated by Simulink.</p> <p>Setting Automatically handle rate transition for data transfer to <i>Always</i> allows Simulink to automatically handle rate transitions by inserting a Rate Transition block. The following exceptions apply:</p> <ul style="list-style-type: none"> • The insertion of a Rate Transition block requires rewiring the block diagram. • Multiple Rate Transition blocks are required: <ul style="list-style-type: none"> • The blocks' sample times are not integer multiples of each other • The blocks use different sample time offsets • One of the rates is asynchronous • An inserted Rate Transition block can have multiple valid configurations. <p>For these cases, manually insert a Rate Transition block or blocks.</p> <p>MathWorks does not recommend using Unit Delay and Zero Order Hold blocks for handling rate transitions.</p>	
Last Changed	R2011a	

ID: Title	cgsl_0205: Signal handling for multirate models
Examples	<p>Not Recommended:</p> <p>In this example, the Rate Transition block is inserted at the source, not at the destination of the signal. The model fails to update because the two destination blocks (Gain and Sum) run at different rates. To fix this error, insert Rate Transition blocks at the signal destinations and remove Rate Transition blocks from the signal sources. Failure to remove the Rate Transition blocks is a common modeling pattern that might result in errors and inefficient code.</p>  <p>Recommended:</p> <p>In this example, the rate transition is inserted at the destination of the signal.</p> 

cgsl_0206: Data integrity and determinism in multitasking models

ID: Title	cgsl_0206: Data integrity and determinism in multitasking models	
Description	For multitasking models that are deployed with a preemptive (interruptible) operating system, protect the integrity of selected signals by doing one of the following:	
	A	Select the Rate Transition block parameter Ensure data integrity during data transfer .
	B	For Inport blocks in Function Called subsystems, select the block parameter Latch input for feedback signals of function-call subsystem outputs .
	To protect selected signal determinism, do one of the following:	
	C	Select the Rate Transition block parameter Ensure deterministic data transfer (maximum delay) .
D	<ul style="list-style-type: none"> • Select the configuration parameter Automatically handle rate transition for data transfer. • Set configuration parameter Deterministic data transfer to Whenever possible or Always. 	
Prerequisites	cgsl_0205:Signal handling for multirate models on page 3-12	
Rationale	A,B, C,D	Following this guideline protects data against possible corruption of preemptive (interruptible) operating systems.
Note	<p>Multitasking systems with a non-preemptive operating system do not require data integrity or determinism protection. In this case, clear these parameters:</p> <ul style="list-style-type: none"> • Rate Transition block parameter Ensure data integrity during data transfer • Configuration parameter Ensure deterministic data transfer (maximum delay) <p>Ensuring data integrity and determinism requires additional memory and execution time. To reduce this additional expense, evaluate signals to determine the level of protection that they require.</p>	
See Also	<ul style="list-style-type: none"> • Rate Transition • “Data Transfer Problems” (Simulink Coder) 	
Last Changed	R2011a	

Configuration Parameter Considerations

- “cgsl_0301: Prioritization of code generation objectives for code efficiency” on page 4-2
- “cgsl_0302: Diagnostic settings for multirate and multitasking models” on page 4-3

cgsl_0301: Prioritization of code generation objectives for code efficiency

ID: Title	cgsl_0301: Prioritization of code generation objectives for code efficiency	
Description	Prioritize code generation objectives for code efficiency by using the Code Generation Advisor.	
	A	Assign priorities to code (ROM, RAM, and Execution efficiency) efficiency objectives.
	B	Select the relative order of ROM, RAM, and Execution efficiency based on application requirements.
	C	Configure the Code Generation Advisor to run before generating code by setting the Check model before generating code configuration parameter to On (proceed with warnings) or On (stop for warnings).
Notes	<p>A model's configuration parameters provide control over many aspects of generated code. The prioritization of objectives specifies how configuration parameters are set when conflicts between objectives occur.</p> <p>Prioritizing code efficiency objectives above safety objectives may remove initialization or run-time protection code (for example, saturation range checking for signals out of representable range). Review the resulting parameter configurations to verify that safety requirements are met.</p>	
Rationale	A, B, C	When you use the Code Generation Advisor, configuration parameters conform to the objectives that you want and they are consistently enforced.
See also	<ul style="list-style-type: none"> • “Application Objectives Using Code Generation Advisor” (Simulink Coder) • “Manage Configuration Sets for a Model” in the Simulink documentation 	
Last Changed	R2015b	

cgsl_0302: Diagnostic settings for multirate and multitasking models

ID: Title	cgsl_0302: Diagnostic settings for multirate and multitasking models
Description	<p>For multirate models using either single tasking or multitasking, set these configuration parameters to warning or error:</p> <ul style="list-style-type: none"> • Single task rate transition • Enforce sample time specified by Signal Specification blocks • Detect multiple driving blocks executing at the same time step <p>For multitasking models, set these configuration parameters to warning or error:</p> <ul style="list-style-type: none"> • Multitask task rate transition • Multitask conditionally executed subsystem • Tasks with equal priority <p>If the model contains Data Store Memory blocks, set these configuration parameters to Enable all as warnings or Enable all as errors:</p> <ul style="list-style-type: none"> • Detect read before write • Detect write after read • Detect write after write • Multitask data store
Rationale	Setting diagnostic configuration parameters improves run-time detection of rate and tasking errors.
See Also	<ul style="list-style-type: none"> • “Model Configuration Parameters: Diagnostics” • “hisl_0013: Usage of data store blocks” • “hisl_0044: Configuration Parameters > Diagnostics > Sample Time” • “hisl_0303: Configuration Parameters > Diagnostics > Data Validity > Merge blocks”
Last Changed	2016a

